CLAIMS

1. A processing arrangement for a computer, the arrangement comprising:

first processor means which is operable to process instructions from a first set of instructions; and

second processor means which is operable to process instructions from a second set of instructions, which second set of instructions is a subset of the first set of instructions, the second processor means being arranged to receive instructions and to process the received instructions independently of the first processor means, when the received instructions form at least part of the second set of instructions.

2. An arrangement as claimed in claim 1, wherein the first processor means includes a plurality of registers, and the second processor means is operable to access a predetermined selection of the said registers.

3. An arrangement as claimed in claims 1 or 2 , wherein the first processor means has active and inactive states of operation, and wherein the second processor means is operable to process instructions when the first processor means is in the inactive state.

4. An arrangement as claimed in claim 3, wherein the second processor means is operable to cause the first processor means to change to the active state from the inactive state, when the received instructions cannot be processed by the second processor means.

5. A processing arrangement as claimed in any one of claims 1 to 4, comprising a plurality of such second processor means for processing respective subsets of the first instruction set.

6. A method of operating a computer including first processor means which operates to process instructions from a first set of instructions, and

second processor means which operates to process instructions from a second set of instructions, which second set of instructions is a subset of the first set of instructions, the method comprising:

using the second processor means to receive instructions; and

processing the received instructions using the second processor means independently of the first processor means when the received instructions form at least a part of said second set of instructions.

7. A method as claimed in claim 6, wherein the first processor means has active and inactive states of operation, and instructions are processed using the second processor means when the first processor means is in the inactive state of operation.